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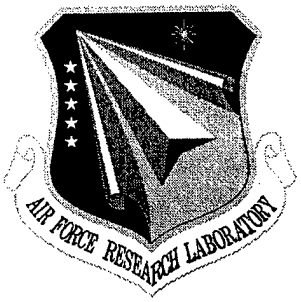

OPTOELECTRONIC MEMORY INTERFACE

California Institute of Technology

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OPTOELECTRONIC MEMORY INTERFACE

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Optoelectronic Memory Interface research involves comparing of read/write holographic memory module with silicon storage, magnetic storage on issue of cost, density, size and speed. With a photorefractive crystal on top of a silicon interface, the holographic memory is of cost efficiency, volume compactness, and fast data accessing. Key challenges to implement the competitive holographic memory are discussed in this report.

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ABSTRACT

This document is a final report on the works of integrated modular holographic memories, in response to the initial proposal 96-31-6, "Optoelectronic memory interface." We compared the read/write holographic memory module with silicon storage, magnetic storage on issues of cost, density, size and speed. With a photorefractive crystal on top of a silicon interface, the holographic memory is of cost efficiency, volume compactness and fast data accessing. Key challenges to implement the competitive holographic memory are discussed.

1. INTRODUCTION

Over the past few decades, the personal computers and the internet have transformed the whole world as people are able to store, retrieve and process more and more information easier and faster. All these benefits inspire more scientific researches on faster, smaller, cheaper and more powerful computer and memory system. Semiconductor electronics have been and will continue to be the driving force in this effort. According to the National Technology Roadmap For Semiconductors 1997(NTRS97),[1] the semiconductor industry has maintained a 25-30% per-year cost reduction per function and the average 10.5%/year reduction rate in feature size throughout its history. It is projected to keep this historic trend for another decade until it reaches physical limits as feature sizes approach 100nm. The magnetic storage density of over 10 Gbits/in^2 is commercially available and keeps pushing to the micro-magnetic limit.

With a photorefractive crystal sitting on top of silicon, a read/write holographic memory is a potential competitive technique to store more data with faster data access, smaller silicon area, lower cost and smaller volume, compared with the traditional silicon Dynamic Random Access Memory (DRAM). Instead of storing data on the silicon area, pages of data are stored as holograms inside the same crystal volume. The silicon devices are only interfaces to read/write holograms to the memory.

Due to the intrinsic parallelism of the holographic memory and the use of silicon interface output, the recording and accessing bandwidths of holographic memory are comparable with silicon DRAM, far more faster than the magnetic storage. Therefore we will concentrate on the DRAM performance as the comparison target for the integrated modular holographic memory.

In section 2, we will discuss the properties of the holographic memory. Section 3 will compare the holographic memory with the silicon memory on issues of cost, density, size and speed. The challenges to the device development, material research and algorithm of data organization for implementing a competitive holographic memory system are addressed.

2. A HOLOGRAPHIC MEMORY SYSTEM

In a holographic memory, a page of data is recorded as phase gratings by interference between the spatial modulated signal beam and a coherent reference beam inside a photorefractive crystal such as $LiNbO_3$, $BaTiO_3$, etc. When the identical reference beam is brought back, the signal wavefront is reconstructed by the diffraction and recovers the data. A large number of different holograms can be recorded in the same

volume of a photorefractive material by angle, spatial, fractal, wavelength, phase coding, peristrophic or shift multiplexing. This leads to a very high data storage density in a crystal. If we assume each page of data has N by N binary pixels and M pages recorded in a crystal of volume V, then we will have storage density MN^2/V bits per volume. Typically $N=10^3$, $M=10^3$ and $V=1$ cm^3, yielding a density of 10^9 bits/cm^3.

Two compact holographic memory designs with different detectors are shown in Figure 1. Different pages of data are angle multiplexed by a laser diode (LD) array. A different one LD is chosen to record and reconstruct one corresponding data page. The switching speed from one page to another can be as fast as 10 microseconds. After being collimated, the beam is separated into two branches. The signal branch goes through Spatial Light Modulator (SLM) or Dynamic Holographic Refresher (DHR) before entering the crystal. Instead of the identical reference beam, the phase conjugate of the reference beam is used for the reconstruction of the signal beam. The volume grating diffraction reconstructs the phase conjugate signal beam, which travels backward and self-focuses back to the original location of the SLM.

The phase conjugate reference beam is achieved by reflection of plane wave reference beams. For each LD cell, there is another cell symmetric to the optical axis of the collimating lens, which constructs the conjugate beam in the crystal by reflection. Compared with using a real phase-conjugate mirror, using a flat mirror is easy, compact and efficient. Simulation indicates that as long as the reference wavefront is a plane wave within one-tenth of a wavelength, we can get up to 90% percent diffraction efficiency using conjugate readout compared to the conventional architecture.

To detect the reconstructed signal, we can deflect the signal to a detector array with a beamsplitter as in Figure 1 (b). The detector cell has the same physical size as the SLM pixel and is aligned pixel to pixel with the SLM image.

Another method is to design a photo sensor cell next to each SLM pixel on the same chip, which leads to the idea of the DHR chip.[2] With the phase conjugate reconstruction, the image of each pixel is self-aligned to its photo sensor, as shown in Figure 1 (a). This makes the system easier to operate and more reliable, at the expense of data page density because of larger area for each cell to contain both the deflector and the sensor.

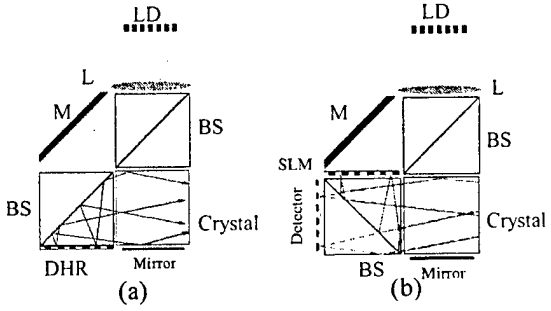


Figure 1. Architectures of phase conjugate holographic memory with (a) DHR chip; (b) separated SLM and detector array. Crystal.: photorefractive crystal; BS: Beam Splitter; M: Mirror; L: Lens.

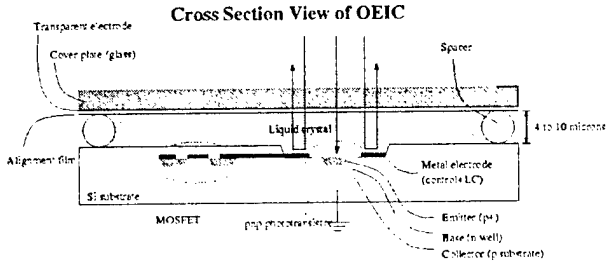


Figure 2. The cross section of Opto-Electronic IC, a DHR cell including a liquid crystal controlled reflector and a photo sensor.

Figure 3. The conjugate reconstruction of 25 holograms by the DHR chip. 1) hologram #1 after 1 cycle recording; 2),3),4) hologram #1,#13,#25 after 100 cycle of refreshing.

Figure 2 shows the cross section of one cell in a DHR chip. Each cell is of 132x211 μm^2, containing a liquid crystal controlled reflector and a photo sensor. DHR chips are fabricated with 24 by 20 cells on a medium size chip by 2 μm process. Figure 3 shows the experimental results of recording, reconstructing and refreshing the holograms in a phase conjugate system with the DHR chip.

Figure 4 shows a model of the holographic memory module with a DHR chip, where LD array is not included. In this module, one 1x1x1 cm^3 LiNbO3 crystal is used as storage medium on top of a 1x1 cm^2 silicon interface. With aggressive projection of one microns dimension for each SLM and Detector pixel, this system can store 50 Gbits on 500 pages. Each page contains 10,000 by 10,000 binary pixels.

We assume that 100 photons are collected for each pixel to have a reasonable SNR detection. To achieve the accessing time 25 μs for each page, it requires a reconstructed power of 0.16 mW. For a material with M/10, the readout reference beam intensity must be at least 0.4W. This will give the data accessing bandwidth as 4 Terabit/sec for each module. At present, a readout time of 250 μsec is feasible given the power available from LDs.

Silicon (1x1 cm^2)	\$125
$LiNbO_3$ (1x1x1 cm^3)	\$10
Liquid Crystal	\$5
Beamsplitters and lens	\$6
LD array (500)	\$25 – 100
Total:	\$171 – 246

Table 1. The estimated cost of each component in a holographic memory module.

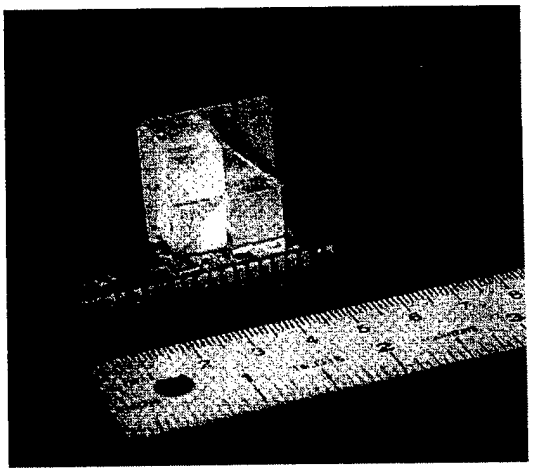


Figure 4. A practical model of a phase conjugate holographic memory module. It includes a DHR chip, one $LiNbO_3$ crystal, two beamsplitters and two mirrors.

3. COMPARING WITH SILICON STORAGE

To build a holographic memory competitive with silicon storage, it is essential to be more cost-efficient, faster data accessing and smaller in volume. We will discuss these issues respectively and address the advantages and drawbacks of the holographic module.

1. Cost model

For the holographic module, the cost includes mainly three parts: silicon interface C_{Si}, optical elements C_{Opt} and LD array C_{LD}, where the LD cost is the most uncertain element. The cost for the optical elements is well known. To compare with the cost of silicon storage DRAM, which is proportional to the silicon area, we assume the same cost for the same silicon area in both holographic memory and DRAM. The cost ratio per megabyte CR of holographic memory to the silicon storage will be:

$$CR = \frac{C_{Si} + C_{Opt} + C_{VCSEL}}{C_{Si}} \cdot \frac{R}{M} \qquad (1)$$

where the R is the pixel area ratio of the SLM and detector to the silicon area of each bit on DRAM, M is the number of holograms multiplexed in the crystal on top of the silicon. With the fixed cost of silicon area

C_{Si}, optical elements C_{Opt}, and LD array C_{LD}, the key to have a small cost ratio CR is to have small R and large M, which means a high storage density in holographic memory comparing with the DRAM.

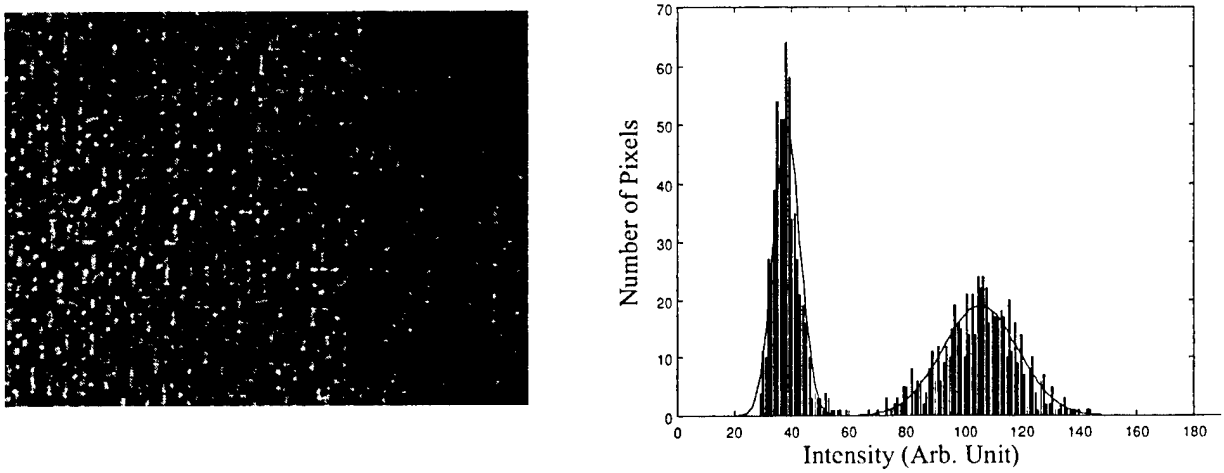
The number of holograms to be recorded and readout with reasonable bit error rate, is limited by the dynamic range and sensitivity, or the M/# of the material.[3] With M holograms recorded with exponential schedule to keep each hologram the same intensity, the diffraction efficiency of each hologram would be:

$$\eta = \left(\frac{M/\#}{M} \right)^2 \qquad (2)$$

Recording and reading 10,000 holograms at one location of a $LiNbO_3$ crystal was demonstrated with a similar system.[4] However limited by the material M/# and the LD array number and power, it is practical to keep M below 1000.

For current commercial SLM and detector array, the pixel area is typically $4x4\mu m^2$. And the current commercial DRAM is 1 μm^2/bit,[1] which leads R=16. With typical M=1000, we have R/M=1.6%, which leads to a small and promising CR. However if the DRAM keeps the history trend as the NTRS97 projected, the DRAM cell will be $0.04\mu m^2$/bit in 2006. To keep the R around 25, the pixel size of the holographic data pages has to be $1x1\mu m^2$ or even smaller, which is achievable for the holographic memory system.

Figure 5 shows the experimental demonstration of the recording and reconstruction of 1x1 μm^2 random pixel mask as SLM. The phase conjugate reconstruction magnified by a x80 microscope is shown in Figure 5 a). The intensity histogram in Figure5 b) is sampled within a 30x30 super-pixel region, which gives Bit Error Rate (BER) at $7x10^{-5}$. This finite BER indicates the requirement for error correction coding for the holographic memory.



a) b)

Figure 5. a) A phase conjugate reconstruction of the random 1x1 μm^2 pixels. b) The intensity histogram for the reconstruction and the Gaussian fitting. SNR=4.8, and BER=$7x10^{-5}$.

Comparing the cost per megabyte for the DRAM projection of 42 cents/Mbyte in 2006, we have the cost estimation for the holographic module in table 1, where we assume the same cost per area for silicon usage. With the R=25 for $1x1\mu m^2$ pixel size and M=500, the cost for holographic memory is around 4 cents/Mbyte, one order of magnitude lower than the DRAM in 2006.

However, if the DRAM feature size keeps decreasing beyond $0.04\mu m^2$/bit with the historic trend, the holographic memory would not be able to follow the pixel size decreases. The pixel size of $1x1\mu m^2$ is

already approaching the physical limit of the wavelength of the light. Therefore with the increasing ratio R, holographic memory will lose its edge comparing with the silicon storage.

A key challenge to the small pixel size is to develop high resolution SLM and detector array to achieve the pixel size as small as 1x1 μm^2.

2. Volume Density

The volume density comparison is similar to the cost model.[5,6] For the previous holographic memory module, the silicon surface density will be up to 440 bits/μm^2 due to the multiplexing M=500 and R=25, which is M/R times higher than the projected DRAM density 22 bits/μm^2 in 2006. For matching the capacity of a holographic module with certain silicon area, as much as M/R times silicon area are needed for conventional silicon storage. These silicon area can be either fabricated on one silicon chip, or on several chips, or combined on several layer by flip chip interconnect. With a factor M/R >20, the holographic memory is expected to have a more compact volume than the silicon storage system.

3. Read/Write Speed

A holographic memory has a large writing and reading speed due to the intrinsic parallelism during recording and reconstructing one full page of data each time. The data transfer rate is N^2/τ, where τ is either the reading time τ_R or the recording time τ_W for one page of data. For the previous holographic module, $N=10^4$, and τ_R=25μs, τ_W=100μs, it has reading rate at $4x10^{12}$ bits/sec and writing rate at 10^{12}bits/sec. Comparing with the projected 16Gbit-DRAM on a 790 mm^2 silicon chip in 2006, which will have 1GHz clock and 2000 pins, DRAM has a maximum read/write rate at $2x10^{12}$ bits/sec. The holographic memory has faster accessing rate and compatible writing rate, although the latency for each page is relatively slow.

To increase the data transport speed, it is essential to increase the number of pixels in each page and decrease the reading/writing time for each page. Both are limited by the power output from the LD array and the M/# of the material. With higher power output and/or higher M/#, it can support a larger data page and decreases the reading and recording time τ_R, τ_W. For the previous holographic module with M/10 and the reading rate at 25 μs for 10^8-pixel-page, it requires the LD array output power as 0.4 W for each, which is achievable for the LD array.

Another drawback for the holographic memory is the disparity between the recording speed and the reading speed. The data accessing time depends on the diffraction efficiency of each hologram, or the M/# of the material. Current photorefractive materials give M/# at the order of 1. To achieve fast accesses to 500 pages, it is crucial to find materials of M/# around 10 or higher. For the recording process, the time to record one hologram depends on the sensitivity of the material. Normally the recording speed is slower than the access speed because of low sensitivity.

This raises another challenge to develop the advanced photorefractive material with high M/# and sensitivity. Current research shows promising results on the material M/# and the sensitivity improvement by optimizing the material doping level and processing. Other work on the doubly doped material for holographic memory[7] provides a potential material with high sensitivity, large M/# and nonvolatility during reading process.

4. Random Access

A holographic memory can randomly access any page of data recorded. However it is difficult to write a new page of data onto an old page of data without changing other pages. The old data page has to be erased before recording a new page on it. Experiments demonstrated that one page can be erased independently and a new page is written at the same location without loss of other page of data.[8] However, it is too complicated to implement it into a practical compact holographic memory.

In addition, the holographic grating recorded in the photorefractive material continues to decay during reading and writing of other gratings at the same location. The data needs to be refreshed during the usage to keep it above acceptable threshold intensity. This can be done by readout the page of data and record it back to the original location to enforce the grating. Experiments are done to record 25 holograms and refresh for 100 times, which demonstrated the ability to refresh with the DHR chip.[9] Figure 3 shows the samples of 25 data images stored and after refreshed 100 times. There is no bit error during these refreshing processes.

A natural storage algorithm for the holographic memory is to keep recording new data into new pages while refreshing old pages in a module. When most the pages of data in a module are obsolete, the whole module is erased before reloading remaining data and new data into it. Considering the big capacity for each module, this is inconvenient compared with silicon storage. In addition, the holographic memory processes data in pages of size 100 Megabit, which is also considerable large as a basic data processing unit. Therefore a practical memory system should combine several holographic modules with some silicon storage as buffer. And special algorithms are necessary to organize and manipulate the data structure.

4. CONCLUSIONS

With an optical crystal seating on top of a silicon interface, the integrated modular holographic memory has comparable recording and accessing bandwidth with DRAM technology, which is much faster than the magnetic storage. Compared with silicon DRAM storage, holographic memory has more cost efficiency than the traditional DRAM, and comparable storage density. It also has the shortcomings of low recording speed, long page latency time, error correct coding requirement, random-page recording complication and large data processing unit. A practical and competitive memory system should combine the holographic memory of low cost and large storage capacity with the conventional flexible silicon storage as buffer. To implement this competitive system, four key challenges have to be overcome: high resolution SLM and detector array, high power high density LD array, advanced photorefractive materials and the data organization algorithm.

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